NTP5864N

Advance Information

Power MOSFET

60 V, 62 A, 13 mΩ

Features

- Low $R_{DS(on)}$
- High Current Capability
- Avalanche Energy Specified
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS (T_J = 25°C unless otherwise stated)

Parameter			Symbol	Value	Units
Drain−to−Source Voltage			V_{DSS}	60	V
Gate−to−Source Voltage − Continuous			V_{GS}	±20	V
Gate−to−Source Voltage − Non−Repetitive (t_p = 10 μs)			V_{GS}	±30	V
Continuous Drain Current − $R_{\theta JC}$ (Note 1)	Steady State	T_C = 25°C	I_D	62	A
		T_C = 100°C		44	
Power Dissipation − $R_{\theta JC}$ (Note 1)	Steady State	T_C = 25°C	P_D	107	W
		T_C = 100°C		54	
Pulsed Drain Current	t_p = 10 μs		I_{DM}	247	A
Operating Junction and Storage Temperature			T_J, T_{STG}	−55 to 175	°C
Source Current (Body Diode) Pulsed			I_S	62	A
Single Pulse Drain−to Source Avalanche Energy − (L = 0.1 mH)			EAS	75	mJ
			IAS	40	A
Lead Temperature for Soldering Purposes (1/8” from case for 10 s)			T_L	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Units
Junction−to−Case (Drain) − Steady State (Note 1)	$R_{\theta JC}$	1.4	°C/W
Junction−to−Ambient − Steady State (Note 1)	$R_{\theta JA}$	33	°C/W

1. Surface mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces).

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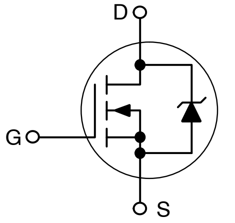
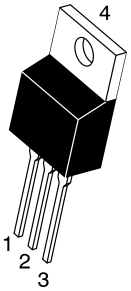
$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	I_D MAX (Note 1)
60 V	13 mΩ @ 10 V	62 A

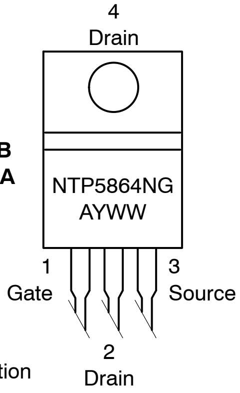
N−Channel



MARKING DIAGRAM & PIN ASSIGNMENT



TO−220AB
CASE 221A
STYLE 5



A = Assembly Location
Y = Year
WW = Work Week
G = Pb−Free Package

ORDERING INFORMATION

Device	Package	Shipping
NTP5864NG	TO−220 (Pb−Free)	50 Units / Rail

June, 2011 − Rev. P2

Publication Order Number:
NTP5864N/D

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise stated)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 μA		60			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$				58		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 60 V	T_J = 25°C			1.0	μA
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V				±100	nA
ON CHARACTERISTICS (Note 2)							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250 μA		2.0		4.0	V
Gate Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$				−10		mV/°C
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 20 A			10.3	13	mΩ
Forward Transconductance	g_{FS}	V_{DS} = 15 V, I_D = 20 A			10		S
CHARGES AND CAPACITANCES							
Input Capacitance	C_{ISS}	V_{GS} = 0 V, f = 1.0 MHz, V_{DS} = 25 V			1640		pF
Output Capacitance	C_{OSS}				190		
Reverse Transfer Capacitance	C_{RSS}				120		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 10 V, V_{DS} = 48 V, I_D = 20 A			30		nC
Threshold Gate Charge	$Q_{G(TH)}$				1.9		
Gate−to−Source Charge	Q_{GS}				7.5		
Gate−to−Drain Charge	Q_{GD}				10		
Gate Resistance	R_g				0.5		Ω
SWITCHING CHARACTERISTICS, V_{GS} = 10 V (Note 3)							
Turn−On Delay Time	$t_{d(ON)}$	V_{GS} = 10 V, V_{DD} = 48 V, I_D = 20 A, R_G = 2.5 Ω			10		ns
Rise Time	t_r				6.4		
Turn−Off Delay Time	$t_{d(OFF)}$				18		
Fall Time	t_f				4.6		
DRAIN−SOURCE DIODE CHARACTERISTICS							
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = 40 A	T_J = 25°C		0.94	1.2	V
			T_J = 125°C		0.84		
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, dI_{SD}/dt = 100 A/μs, I_S = 20 A			24		ns
Charge Time	t_a				15		
Discharge Time	t_b				8.7		
Reverse Recovery Charge	Q_{RR}				20		nC

2. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
3. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

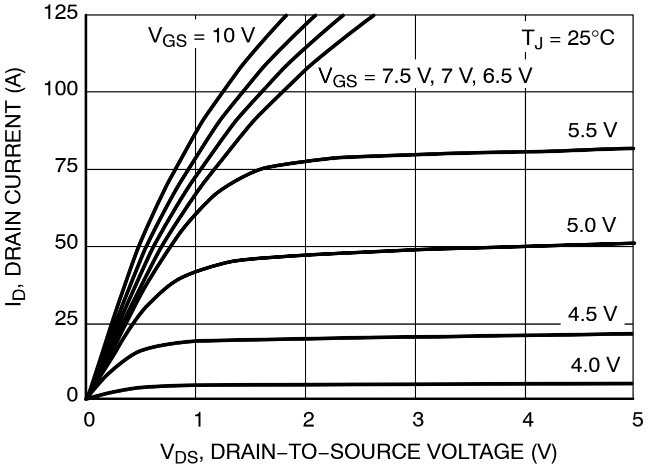


Figure 1. On−Region Characteristics

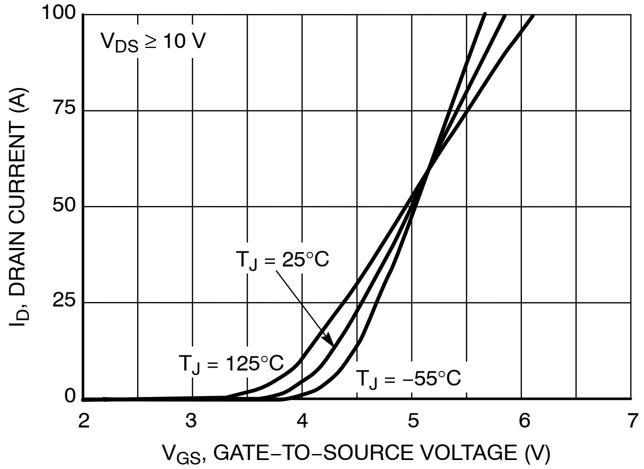


Figure 2. Transfer Characteristics

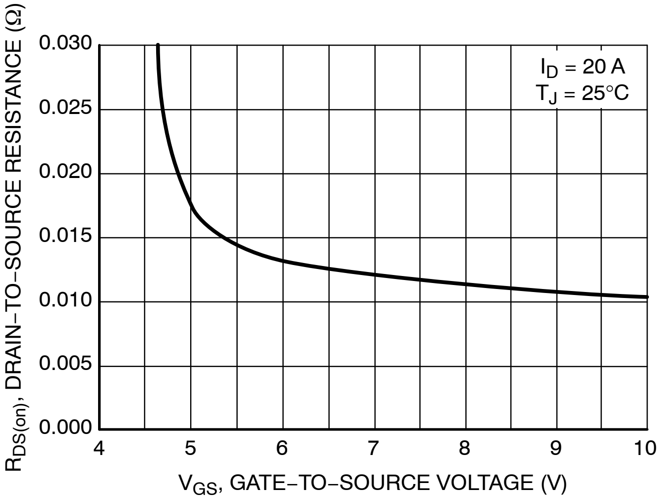


Figure 3. On−Resistance vs. Gate Voltage

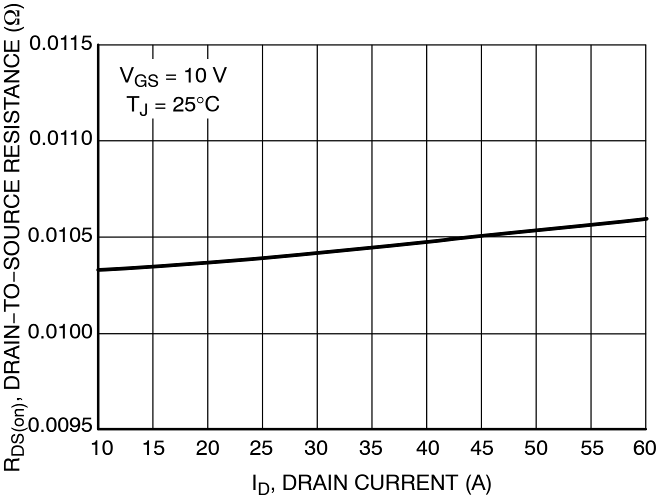


Figure 4. On−Resistance vs. Drain Current

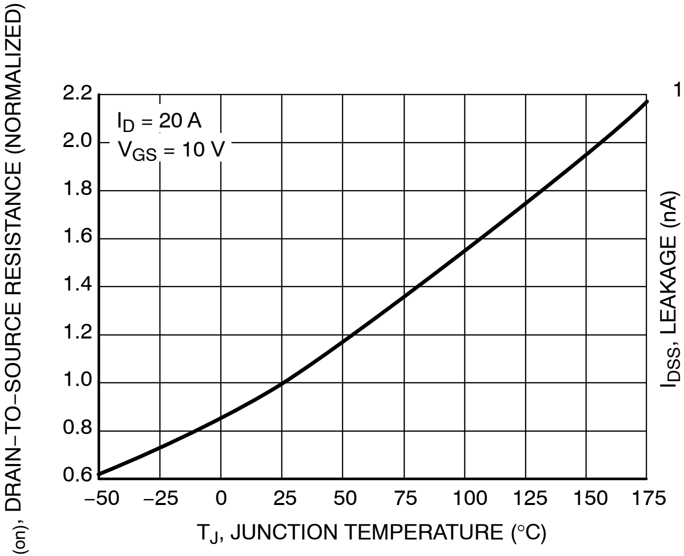


Figure 5. On−Resistance Variation with Temperature

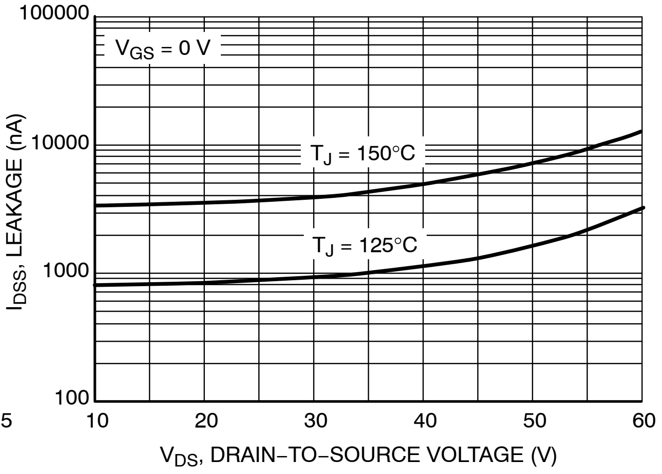


Figure 6. Drain−to−Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

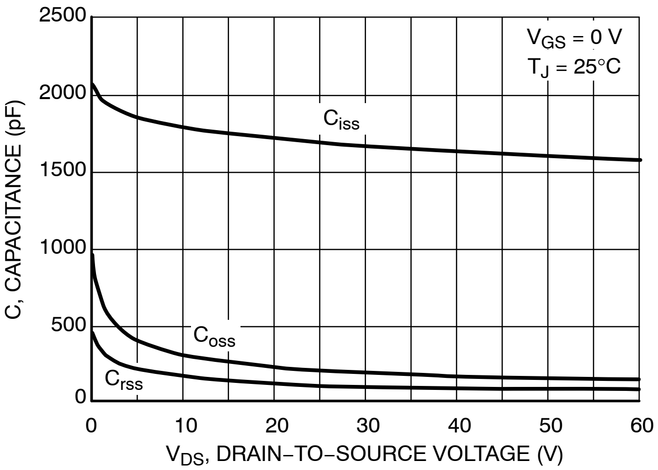


Figure 7. Capacitance Variation

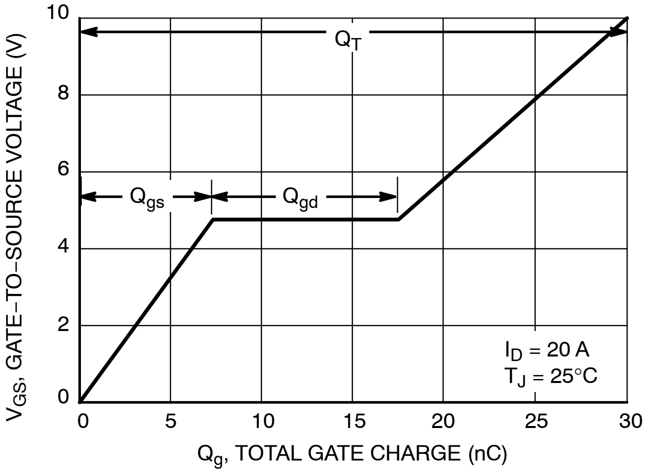


Figure 8. Gate−to−Source vs. Total Charge

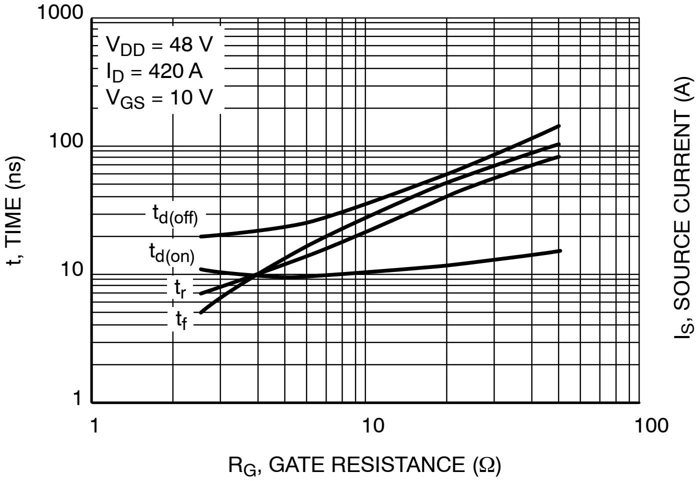


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

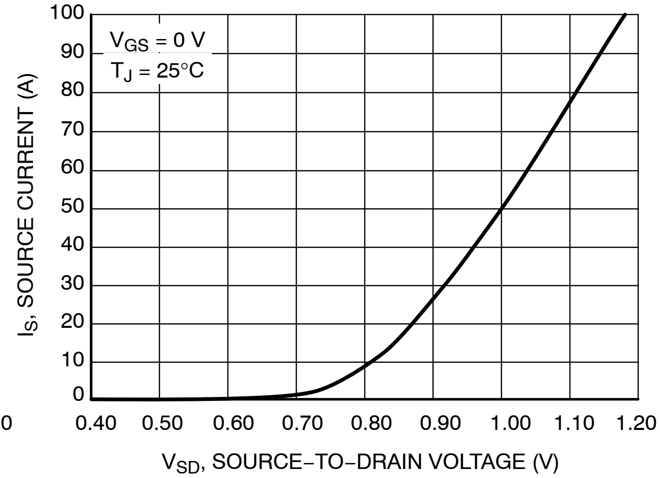


Figure 10. Diode Forward Voltage vs. Current

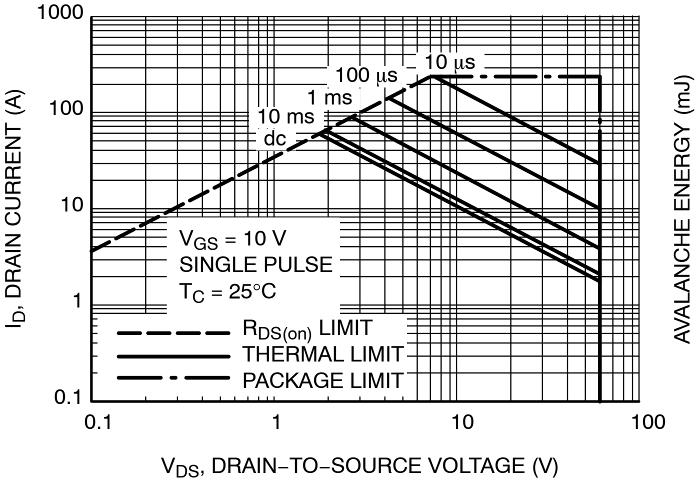


Figure 11. Maximum Rated Forward Biased Safe Operating Area

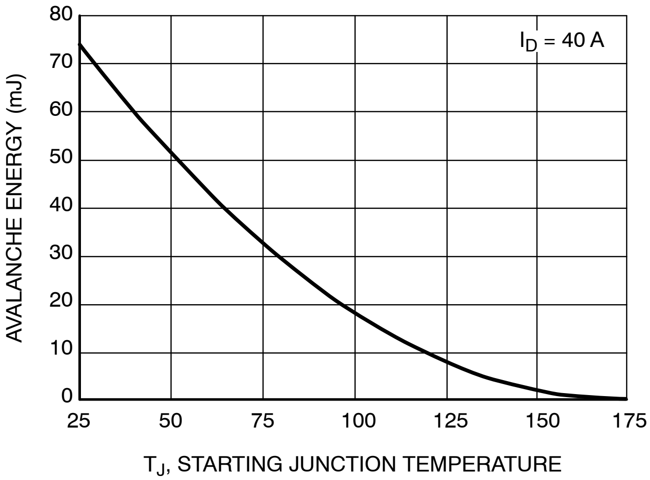


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

TYPICAL CHARACTERISTICS

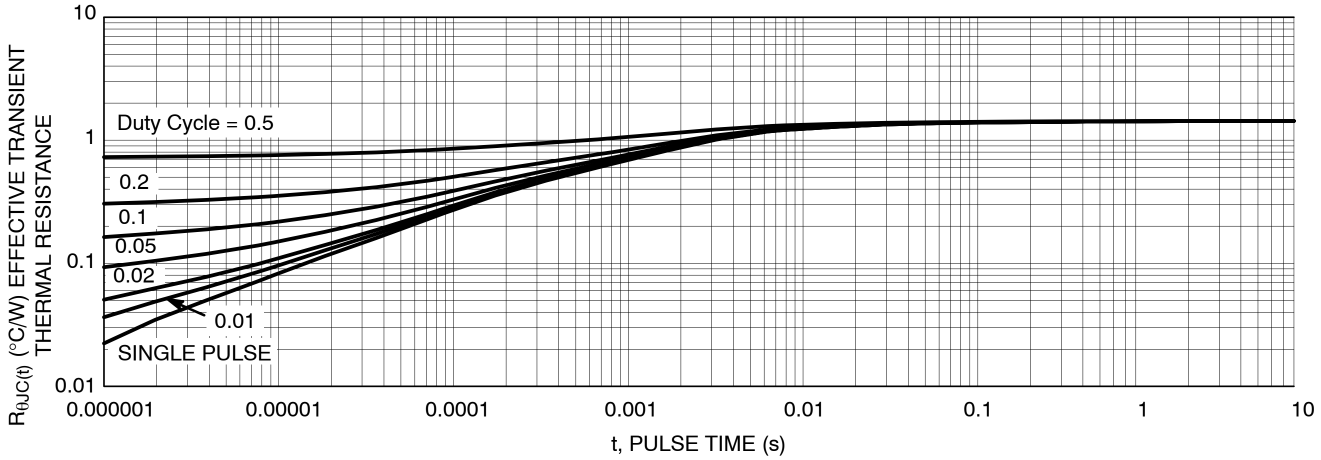
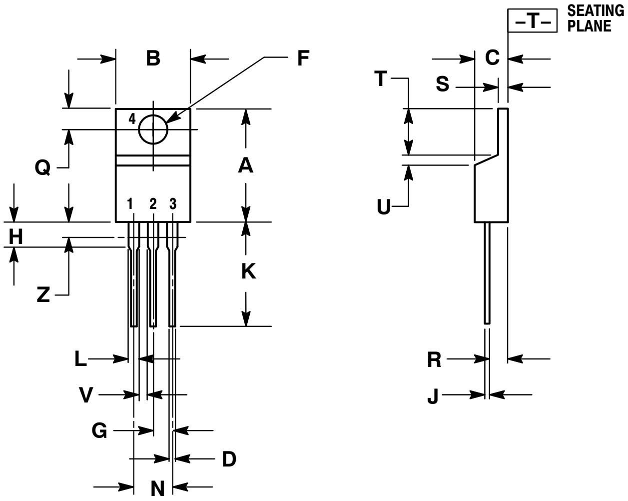


Figure 13. Thermal Response

PACKAGE DIMENSIONS

TO−220

CASE 221A−09
ISSUE AF



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

	INCHES		MILLIMETERS	
DIM	**MIN**	**MAX**	**MIN**	**MAX**
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.161	3.61	4.09
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.014	0.025	0.36	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	−−−	1.15	−−−
Z	−−−	0.080	−−−	2.04

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

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